TEXAS INSTRUMENTS

PCA9555

SCPS131F −AUGUST 2005−REVISED JUNE 2014

PCA9555 Remote 16-Bit I^{2}C and SMBus I/O Expander With Interrupt Output and Configuration Registers

1 Features

- Low Standby-Current Consumption of 1 µA Max
- I^{2}C to Parallel Port Expander
- Open-Drain Active-Low Interrupt Output
- 5-V Tolerant I/O Ports
- Compatible With Most Microcontrollers
- 400-kHz Fast I^{2}C Bus
- Address by Three Hardware Address Pins for Use of up to Eight Devices
- Polarity Inversion Register
- Latched Outputs With High-Current Drive Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Description

This 16-bit I/O expander for the two-line bidirectional bus (I^{2}C) is designed for 2.3-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I^{2}C interface [serial clock (SCL), serial data (SDA)].
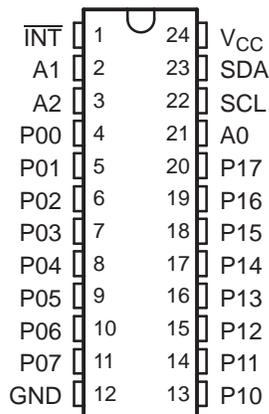
The PCA9555 consists of two 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active high or active low operation) registers. At power on, the I/Os are configured as inputs. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCA9555	SSOP (16)	6.20 mm × 5.30 mm
	VQFN (16)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
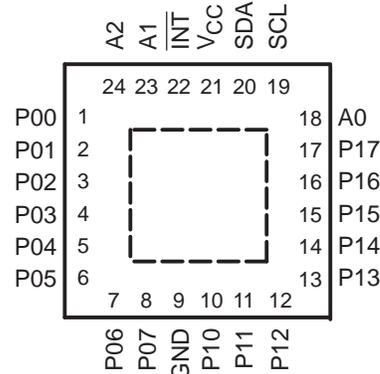
DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)

$\overline{INT}$	1	24	V$_{CC}$
A1	2	23	SDA
A2	3	22	SCL
P00	4	21	A0
P01	5	20	P17
P02	6	19	P16
P03	7	18	P15
P04	8	17	P14
P05	9	16	P13
P06	10	15	P12
P07	11	14	P11
GND	12	13	P10

RGE PACKAGE
(TOP VIEW)

Top pins: A2 (24), A1 (23), $\overline{INT}$ (22), V$_{CC}$ (21), SDA (20), SCL (19)

P00	1	18	A0
P01	2	17	P17
P02	3	16	P16
P03	4	15	P15
P04	5	14	P14
P05	6	13	P13

Bottom pins: P06 (7), P07 (8), GND (9), P10 (10), P11 (11), P12 (12)

Table of Contents

3 Revision History

4   Description (Continued)

The system master can reset the PCA9555 in the event of a timeout or other improper operation by utilizing the power-on reset feature, which puts the registers in their default state and initializes the I²C/SMBus state machine.

The PCA9555 open-drain interrupt ($\overline{\text{INT}}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C bus. Thus, the PCA9555 can remain a simple slave device.

The device outputs (latched) have high-current drive capability for directly driving LEDs.

Although pin-to-pin and I²C-address is compatible with the PCF8575, software changes are required due to the enhancements.

The PCA9555 is identical to the PCA9535, except for the inclusion of the internal I/O pullup resistor, which pulls the I/O to a default high when configured as an input and undriven.

Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I²C address and allow up to eight devices to share the same I²C bus or SMBus. The fixed I²C address of the PCA9555 is the same as the PCF8575, PCF8575C, and PCF8574, allowing up to eight of these devices in any combination to share the same I²C bus or SMBus.

5 Pin Configuration and Functions

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)
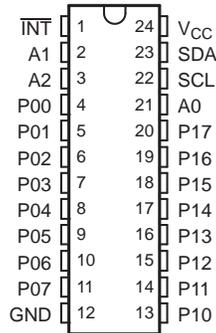
RGE PACKAGE
(TOP VIEW)
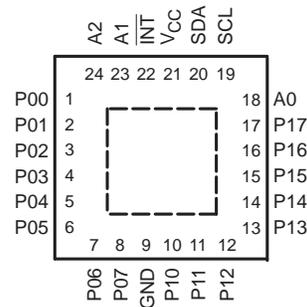
Pin Functions

PIN			DESCRIPTION
NAME	SOIC (D), SSOP (DB), QSOP (DBQ), TSSOP (PW), AND TVSOP (DGV)	QFN (RGE)	
$\overline{\text{INT}}$	1	22	Interrupt output. Connect to V_{CC} through a pullup resistor.
A1	2	23	Address input 1. Connect directly to V_{CC} or ground.
A2	3	24	Address input 2. Connect directly to V_{CC} or ground.
P00	4	1	P-port input/output. Push-pull design structure.
P01	5	2	P-port input/output. Push-pull design structure.
P02	6	3	P-port input/output. Push-pull design structure.
P03	7	4	P-port input/output. Push-pull design structure.
P04	8	5	P-port input/output. Push-pull design structure.
P05	9	6	P-port input/output. Push-pull design structure.
P06	10	7	P-port input/output. Push-pull design structure.
P07	11	8	P-port input/output. Push-pull design structure.
GND	12	9	Ground
P10	13	10	P-port input/output. Push-pull design structure.
P11	14	11	P-port input/output. Push-pull design structure.
P12	15	12	P-port input/output. Push-pull design structure.
P13	16	13	P-port input/output. Push-pull design structure.
P14	17	14	P-port input/output. Push-pull design structure.
P15	18	15	P-port input/output. Push-pull design structure.
P16	19	16	P-port input/output. Push-pull design structure.
P17	20	17	P-port input/output. Push-pull design structure.
A0	21	18	Address input 0. Connect directly to V_{CC} or ground.
SCL	22	19	Serial clock bus. Connect to V_{CC} through a pullup resistor.
SDA	23	20	Serial data bus. Connect to V_{CC} through a pullup resistor.
V_{CC}	24	21	Supply voltage

Product Folder Links: *PCA9555*

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6	V
V_I	Input voltage range [2]		−0.5	6	V
V_O	Output voltage range [2]		−0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		−20	mA
I_{OK}	Output clamp current	$V_O < 0$		−20	mA
I_{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current	$V_O = 0$ to V_{CC}		−50	mA
I_{CC}	Continuous current through GND			−250	mA
	Continuous current through V_{CC}			160	
θ_{JA}	Package thermal impedance, junction to free air [3]	DB package		63	°C/W
		DBQ package		61	
		DGV package		86	
		DW package		46	
		PW package		88	
		RGE package		45	
θ_{JP}	Package thermal impedance, junction to pad	RGE package		1.5	°C/W

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [1]	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins [2]	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	$0.7 \times V_{CC}$	5.5	V
		A2–A0, P07–P00, P17–P10	$0.7 \times V_{CC}$	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	−0.5	$0.3 \times V_{CC}$	V
		A2–A0, P07–P00, P17–P10	−0.5	$0.3 \times V_{CC}$	
I_{OH}	High-level output current	P07–P00, P17–P10		−10	mA
I_{OL}	Low-level output current	P07–P00, P17–P10		25	mA
T_A	Operating free-air temperature		−40	85	°C

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6.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{IK}	Input diode clamp voltage	$I_I = -18$ mA	2.3 V to 5.5 V	−1.2			V
V_{POR}	Power-on reset voltage	$V_I = V_{CC}$ or GND, $I_O = 0$	V_{POR}		1.5	1.65	V
V_{OH}	P-port high-level output voltage[2]	$I_{OH} = -8$ mA	2.3 V	1.8			V
			3 V	2.6			
			4.75 V	4.1			
		$I_{OH} = -10$ mA	2.3 V	1.7			
			3 V	2.5			
			4.75 V	4			
I_{OL}	SDA	$V_{OL} = 0.4$ V	2.3 V to 5.5 V		3		mA
	P port[3]	$V_{OL} = 0.5$ V			8	20	
		$V_{OL} = 0.7$ V			10	24	
	$\overline{INT}$	$V_{OL} = 0.4$ V			3		
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V			±1	µA
	A2–A0					±1	
I_{IH}	P port	$V_I = V_{CC}$	2.3 V to 5.5 V			1	µA
I_{IL}	P port	$V_I = $ GND	2.3 V to 5.5 V			−100	µA
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, $I_O = 0$, I/O = inputs, $f_{SCL} = 400$ kHz, No load	5.5 V		100	200	µA
			3.6 V		30	75	
			2.7 V		20	50	
	Standby mode	Low inputs	$V_I = $ GND, $I_O = 0$, I/O = inputs, $f_{SCL} = 0$ kHz, No load	5.5 V		1.1	1.5	mA
				3.6 V		0.7	1.3	
				2.7 V		0.5	1	
		High inputs	$V_I = V_{CC}$, $I_O = 0$, I/O = inputs, $f_{SCL} = 0$ kHz, No load	5.5 V		0.5	1	µA
				3.6 V		0.4	0.9	
				2.7 V		0.25	0.8	
ΔI_{CC}	Additional current in standby mode	One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V			1.5	mA
C_I	SCL	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V		3	7	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	2.3 V to 5.5 V		3	7	pF
	P port				3.7	9.5	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and $T_A = 25°C$.
(2) Each I/O must be externally limited to a maximum of 25 mA, and each octal (P07–P00 and P17–P10) must be limited to a maximum current of 100 mA, for a device total of 200 mA.
(3) The total current sourced by all I/Os must be limited to 160 mA (80 mA for P07–P00 and 80 mA for P17–P10).

6.5 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 14)

			MIN	MAX	UNIT
t_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		0.6		µs
t_{scl}	I²C clock low time		1.3		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time		$20 + 0.1C_b$ [(1)]	300	ns
t_{icf}	I²C input fall time		$20 + 0.1C_b$ [(1)]	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus	$20 + 0.1C_b$ [(1)]	300	ns
t_{buf}	I²C bus free time between Stop and Start		1.3		µs
t_{sts}	I²C Start or repeated Start condition setup		0.6		µs
t_{sth}	I²C Start or repeated Start condition hold		0.6		µs
t_{sps}	I²C Stop condition setup		0.6		µs
$t_{vd(Data)}$	Valid-data time	SCL low to SDA output valid	50		ns
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA (out) low	0.1	0.9	µs
C_b	I²C bus capacitive load			400	pF

(1) C_b = total capacitance of one bus line in pF

6.6 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see Figure 15 and Figure 16)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4	µs
t_{pv}	Output data valid	SCL	P port		200	ns
t_{ps}	Input data setup time	P port	SCL	150		ns
t_{ph}	Input data hold time	P port	SCL	1		µs

6.7 Typical Characteristics
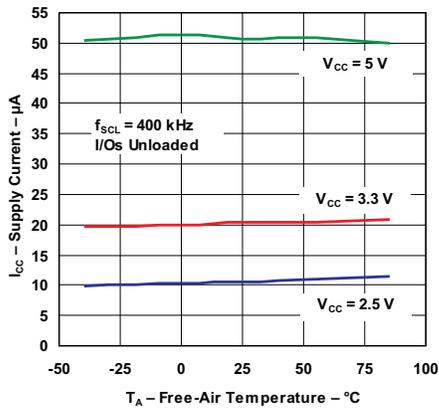
T_A = 25°C (unless otherwise noted)

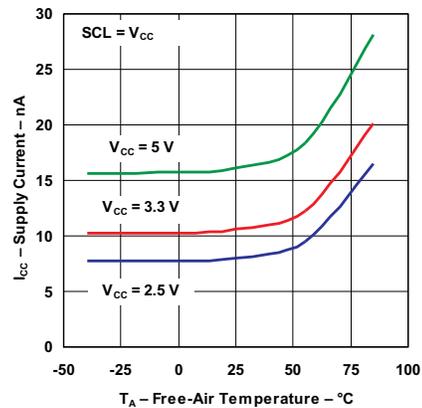Figure 1. Supply Current vs Temperature

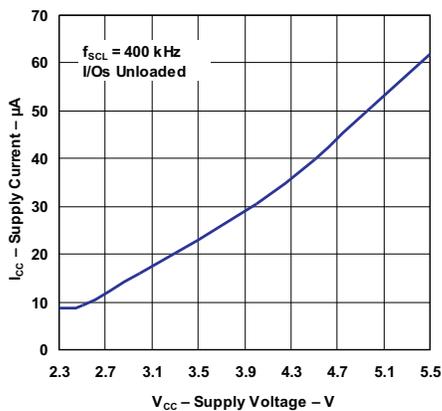Figure 2. Standby Supply Current vs Temperature

Figure 3. Supply Current vs Supply Voltage

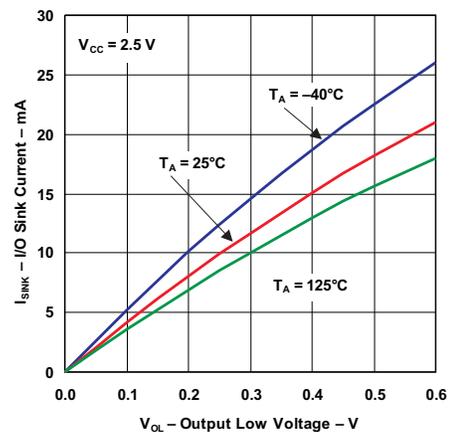

Figure 4. I/O Sink Current vs Output Low Voltage
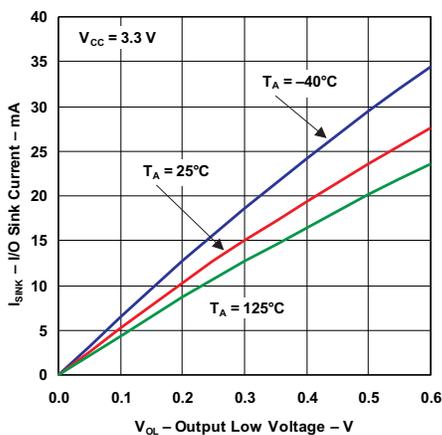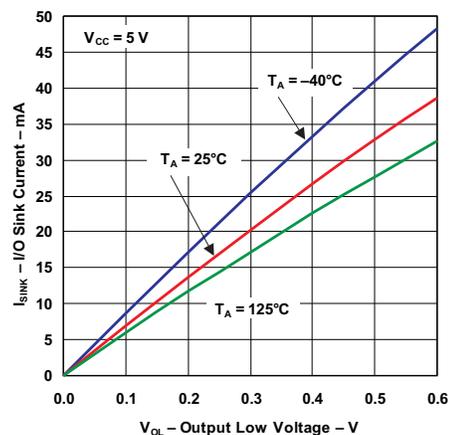

Figure 5. I/O Sink Current vs Output Low Voltage

Figure 6. I/O Sink Current vs Output Low Voltage

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Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)
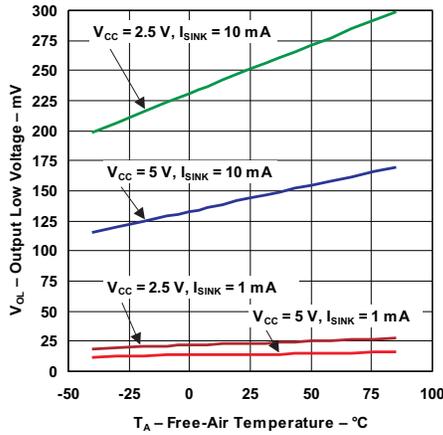
Figure 7. I/O Output Low Voltage vs Temperature
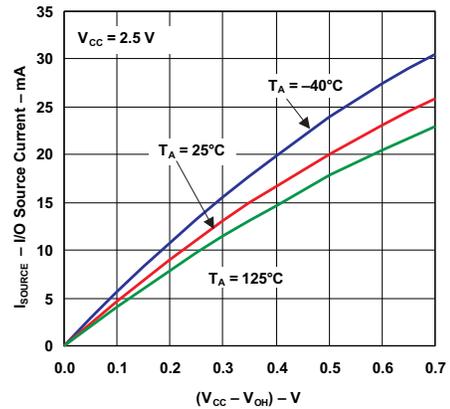
Figure 8. I/O Source Current vs Output High Voltage
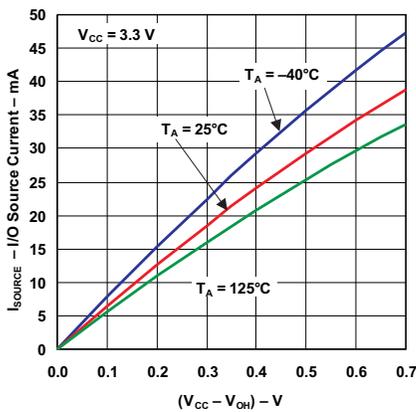
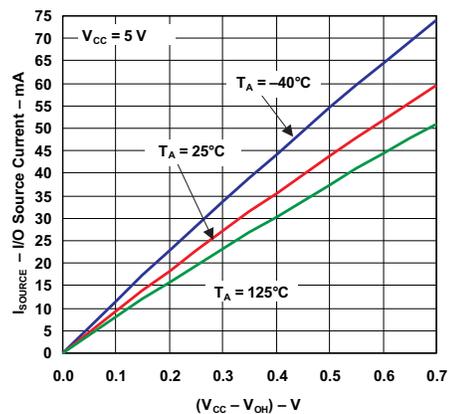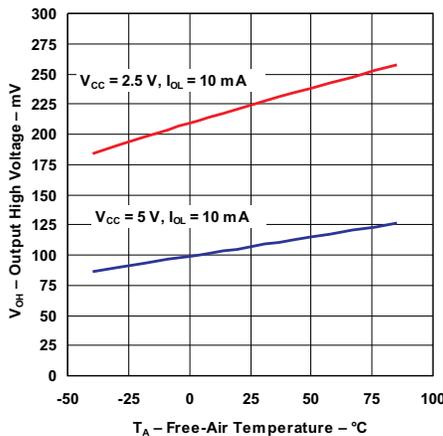**Figure 9. I/O Source Current vs Output High Voltage**

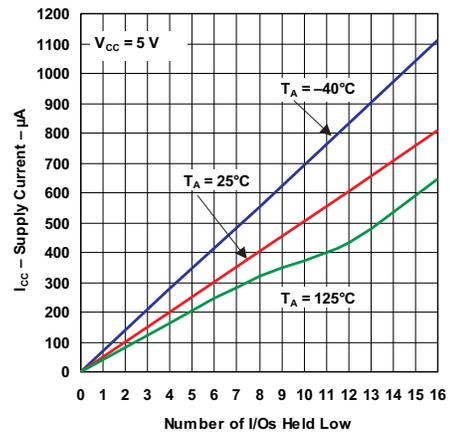**Figure 10. I/O Source Current vs Output High Voltage**

Figure 11. I/O High Voltage vs Temperature

Figure 12. Supply Current vs Number Of I/Os Held Low
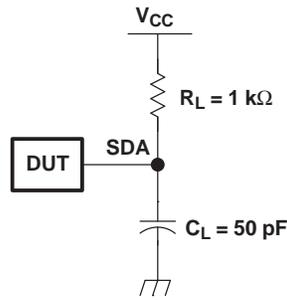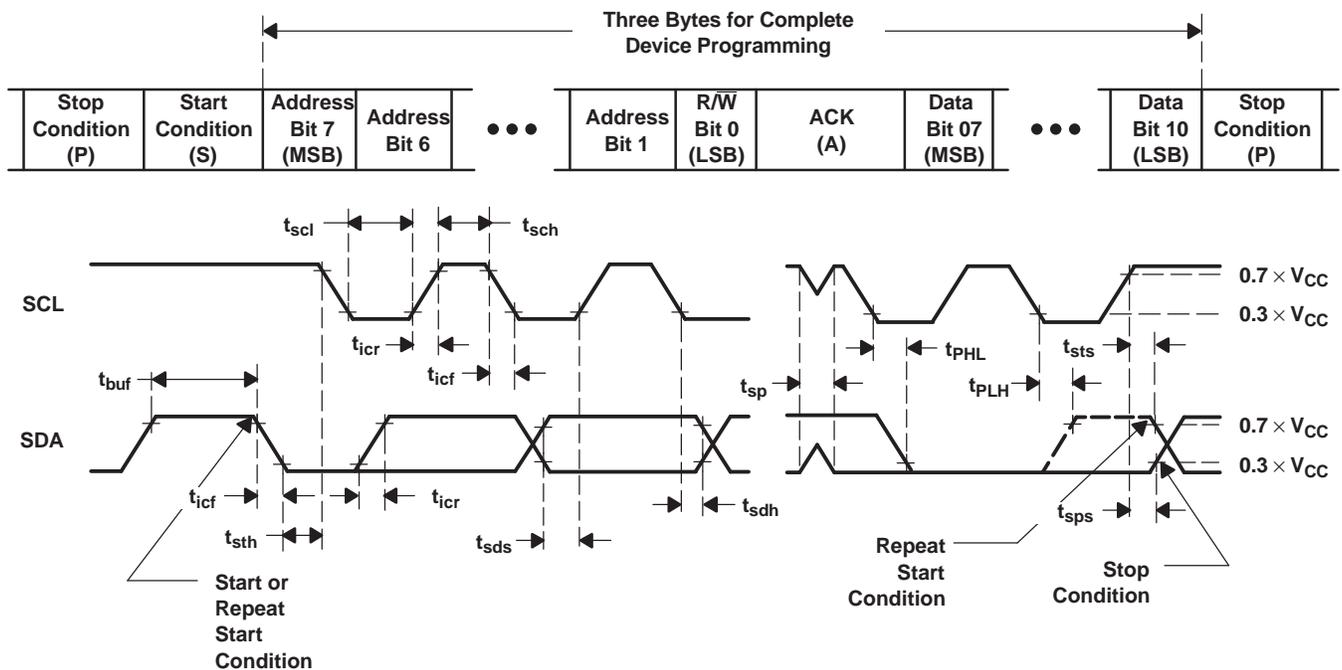
Product Folder Links: *PCA9555*

Typical Characteristics (continued)

$T_A = 25°C$ (unless otherwise noted)
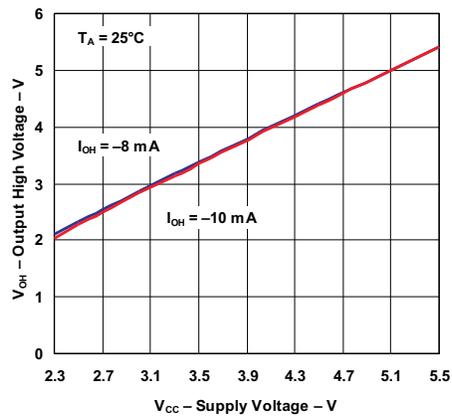
Figure 13. Output High Voltage vs Supply Voltage

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Product Folder Links: *PCA9555*

7 Parameter Measurement Information

SDA LOAD CONFIGURATION

VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

A. C_L includes probe and jig capacitance.

B.   All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C.   All parameters and waveforms are not applicable to all devices.

Figure 14. I^2C Interface Load Circuit And Voltage Waveforms

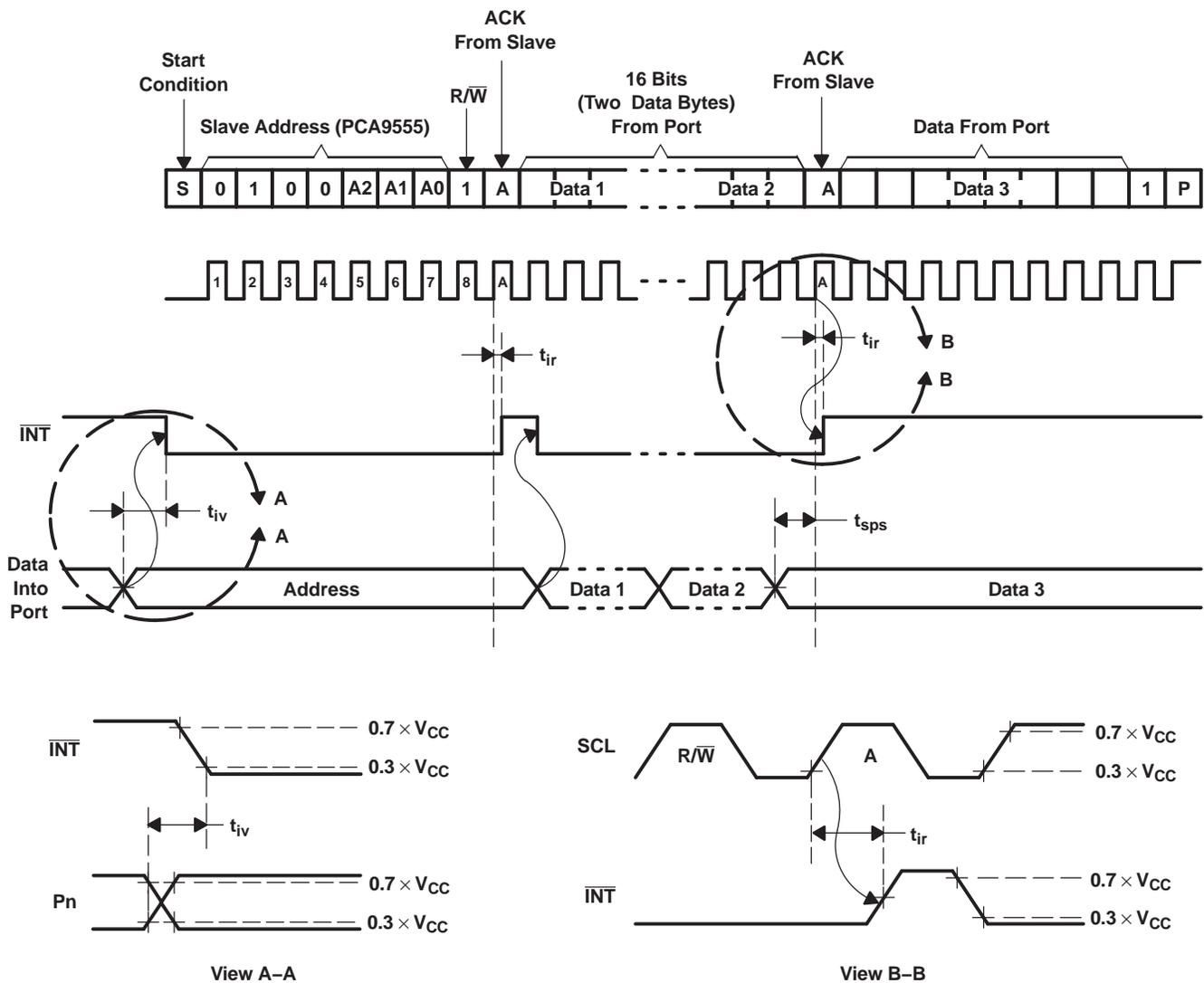## Parameter Measurement Information (continued)
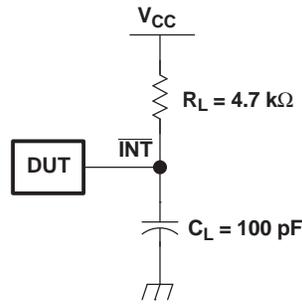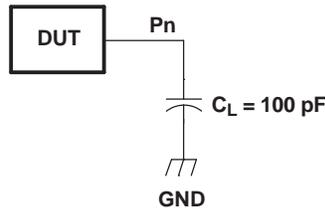

INTERRUPT LOAD CONFIGURATION
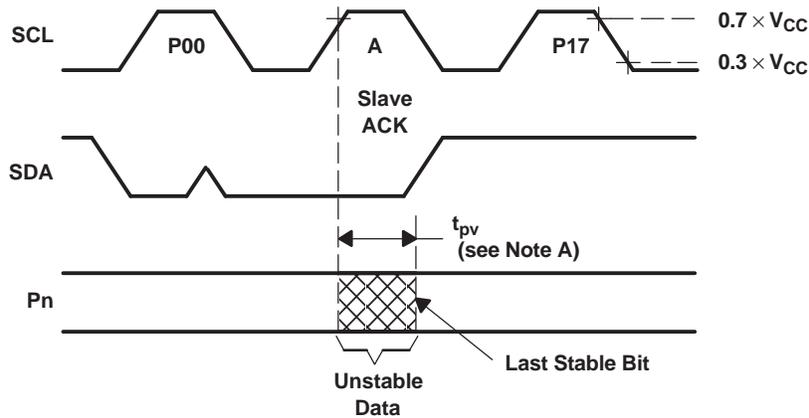

A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. All parameters and waveforms are not applicable to all devices.

Figure 15. Interrupt Load Circuit And Voltage Waveforms

Parameter Measurement Information (continued)

P-PORT LOAD CONFIGURATION

WRITE MODE (R/$\overline{W}$ = 0)
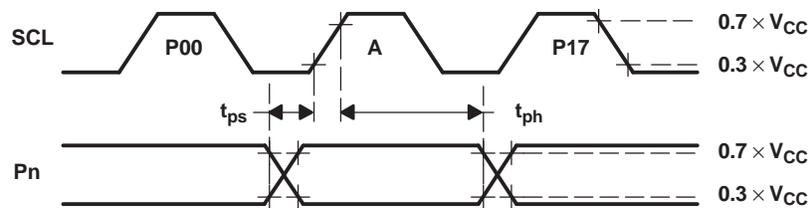
READ MODE (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.

B. t_{pv} is measured from $0.7 \times V_{CC}$ on SCL to 50% I/O (Pn) output.

C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 16. P-Port Load Circuit And Voltage Waveforms

8 Detailed Description

8.1 Functional Block Diagram
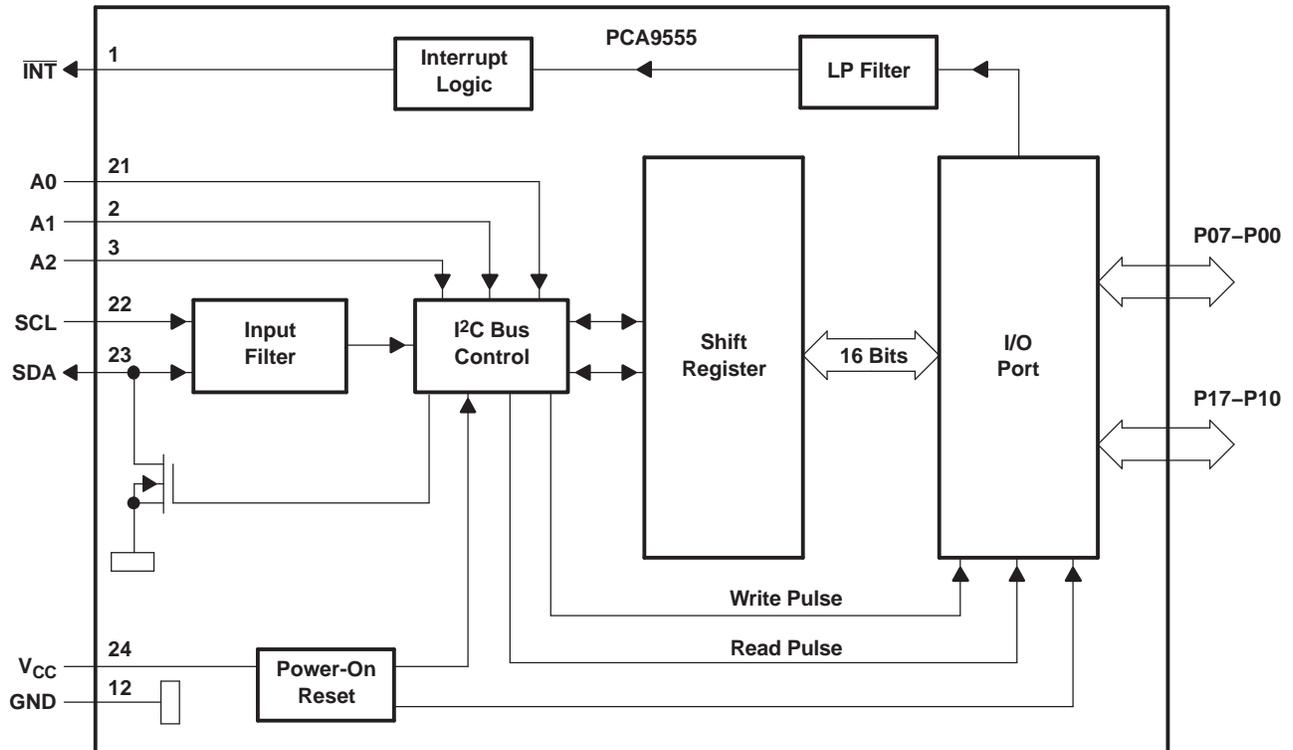
A. Pin numbers shown are for DB, DBQ, DGV, DW, and PW packages.

B. All I/Os are set to inputs at reset.

Figure 17. Logic Diagram

Functional Block Diagram (continued)
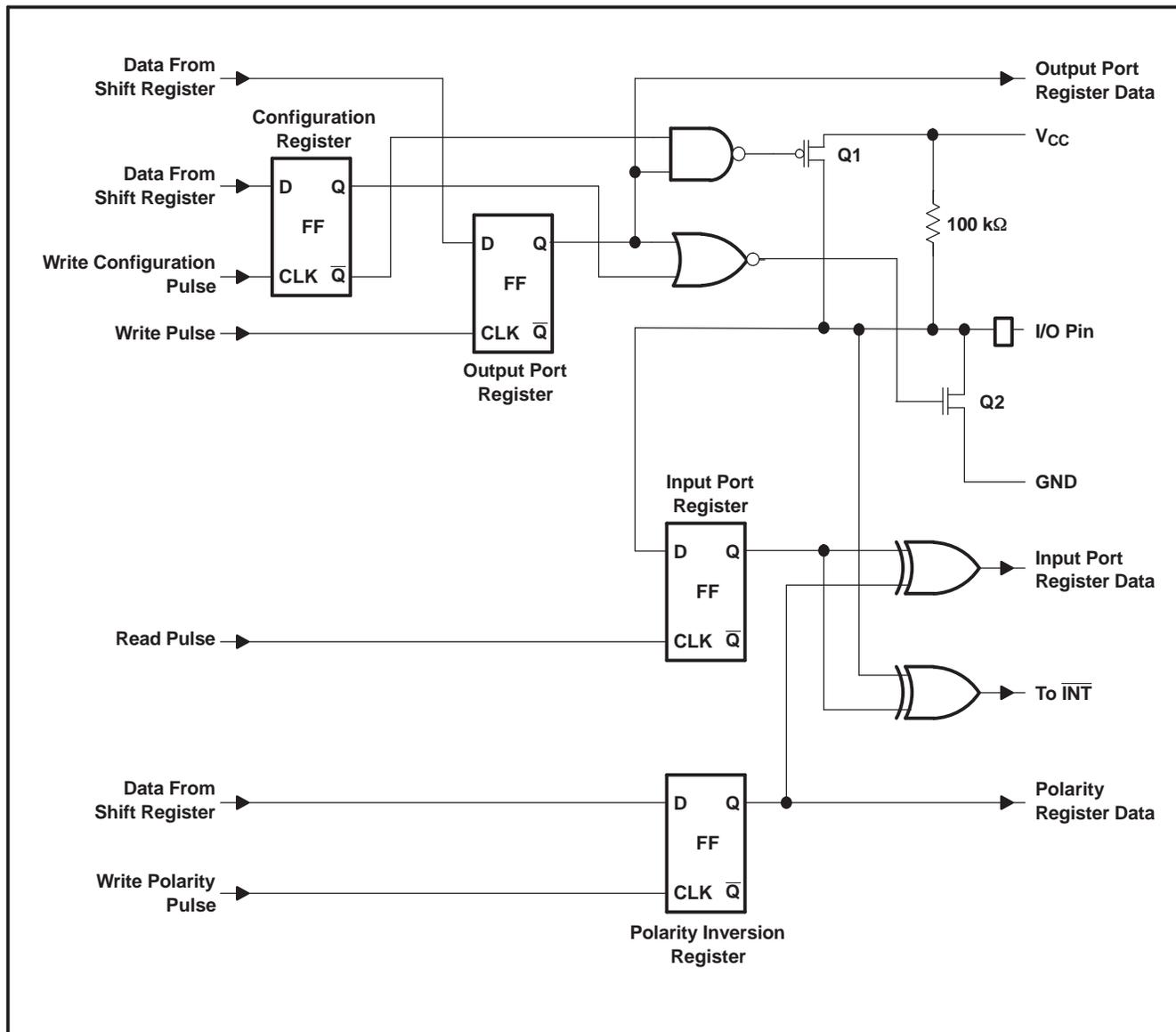
(1)   At power-on reset, all registers return to default values.

Figure 18. Simplified Schematic Of P-Port I/Os

8.2   Device Functional Modes

8.2.1   Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the PCA9555 in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the PCA9555 registers and I²C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

Refer to the *Power-On Reset Errata* section.

Device Functional Modes (continued)

8.2.2 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 (in Figure 18) are off, creating a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output Port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

8.2.3 Interrupt ($\overline{INT}$) Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting, data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$. Writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register. Because each 8-pin port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1 or vice versa.

The $\overline{INT}$ output has an open-drain structure and requires pullup resistor to V_{CC}.

8.2.3.1 Interrupt Errata

Description

The INT will be improperly de-asserted if the following two conditions occur:

1. The last I^2C command byte (register pointer) written to the device was 00h.

> **NOTE**
> This generally means the last operation with the device was a Read of the input register. However, the command byte may have been written with 00h without ever going on to read the input register. After reading from the device, if no other command byte written, it will remain 00h.

2. Any other slave device on the I^2C bus acknowledges an address byte with the R/W bit set high

System Impact

Can cause improper interrupt handling as the Master will see the interrupt as being cleared.

System Workaround

Minor software change: User must change command byte to something besides 00h after a Read operation to the PCA9555 device or before reading from another slave device.

> **NOTE**
> Software change will be compatible with other versions (competition and TI redesigns) of this device.

8.3 Programming

8.3.1 I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 19). After the Start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address.

After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the Start and Stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 20).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 19).

Any number of data bytes can be transferred from the transmitter to the receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 21). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.
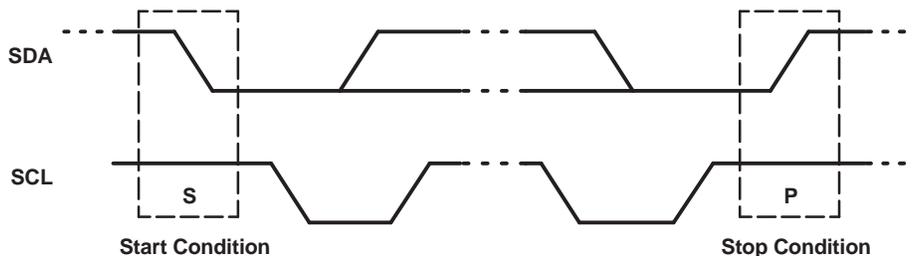
Figure 19. Definition Of Start And Stop Conditions
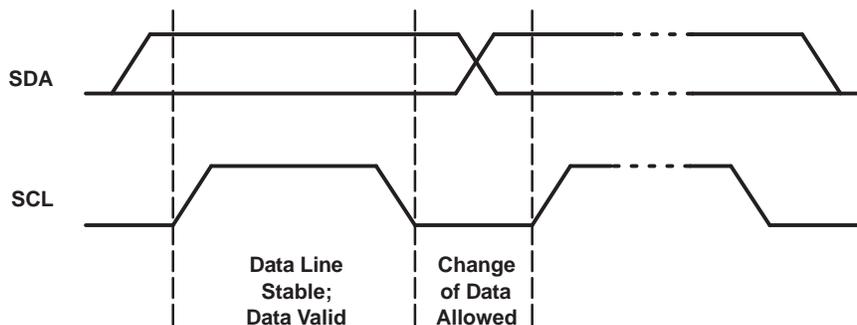
Figure 20. Bit Transfer

Product Folder Links: *PCA9555*

Programming (continued)
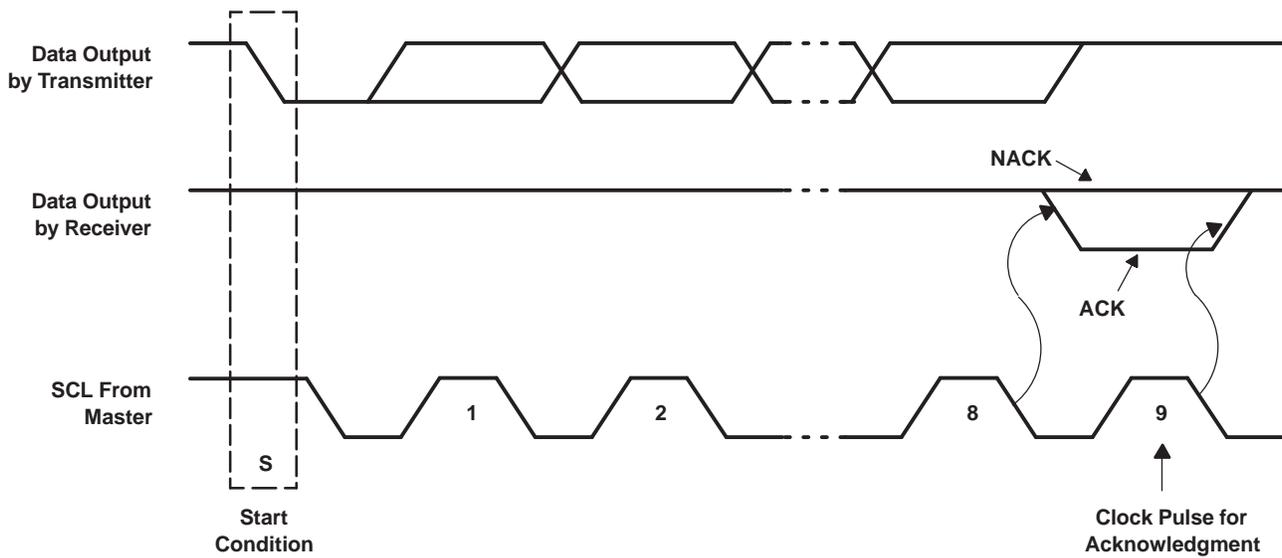
Figure 21. Acknowledgment On I²C Bus

8.3.2 Register Map

Table 1. Interface Definition

BYTE	BIT							
	7 (MSB)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (LSB)**
I²C slave address	L	H	L	L	A2	A1	A0	R/$\overline{W}$
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

8.3.2.1 Device Address

Figure 22 shows the address byte of the PCA9555.
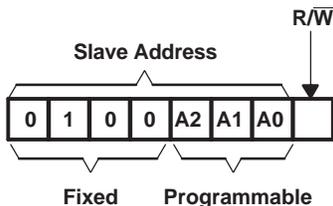
Figure 22. PCA9555 Address

Table 2. Address Reference

INPUTS			I²C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	32 (decimal), 20 (hexadecimal)
L	L	H	33 (decimal), 21 (hexadecimal)
L	H	L	34 (decimal), 22 (hexadecimal)
L	H	H	35 (decimal), 23 (hexadecimal)
H	L	L	36 (decimal), 24 (hexadecimal)
H	L	H	37 (decimal), 25 (hexadecimal)
H	H	L	38 (decimal), 26 (hexadecimal)
H	H	H	39 (decimal), 27 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

8.3.2.2 Control Register And Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the PCA9555. Three bits of this data byte state the operation (read or write) and the internal register (input, output, polarity inversion, or configuration) that will be affected. This register can be written or read through the I²C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.
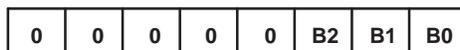
Figure 23. Control Register Bits

Table 3. Command Byte

CONTROL REGISTER BITS			COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B2	B1	B0				
0	0	0	0x00	Input Port 0	Read byte	xxxx xxxx
0	0	1	0x01	Input Port 1	Read byte	xxxx xxxx
0	1	0	0x02	Output Port 0	Read/write byte	1111 1111
0	1	1	0x03	Output Port 1	Read/write byte	1111 1111
1	0	0	0x04	Polarity Inversion Port 0	Read/write byte	0000 0000
1	0	1	0x05	Polarity Inversion Port 1	Read/write byte	0000 0000
1	1	0	0x06	Configuration Port 0	Read/write byte	1111 1111
1	1	1	0x07	Configuration Port 1	Read/write byte	1111 1111

8.3.2.3 Register Descriptions

The Input Port registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to indicate to the the I^{2}C device that the Input Port register will be accessed next.

Table 4. Registers 0 And 1 (Input Port Registers)

Bit	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X
Bit	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

The Output Port registers (registers 2 and 3) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 5. Registers 2 And 3 (Output Port Registers)

Bit	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1
Bit	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

The Polarity Inversion registers (registers 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained.

Table 6. Registers 4 And 5 (Polarity Inversion Registers)

Bit	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0
Bit	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

The Configuration registers (registers 6 and 7) configure the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Table 7. Registers 6 And 7 (Configuration Registers)

Bit	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1
Bit	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

Product Folder Links: *PCA9555*

8.3.2.4 Bus Transactions

Data is exchanged between the master and the PCA9555 through write and read commands.

8.3.2.4.1 Writes

Data is transmitted to the PCA9555 by sending the device address and setting the least-significant bit to a logic 0 (see Figure 22 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte.

The eight registers within the PCA9555 are configured to operate as four register pairs. The four pairs are input ports, output ports, polarity inversion ports, and configuration ports. After sending data to one register, the next data byte is sent to the other register in the pair (see Figure 24 and Figure 25). For example, if the first byte is sent to output port (register 3), the next byte is stored in Output Port 0 (register 2).

There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.
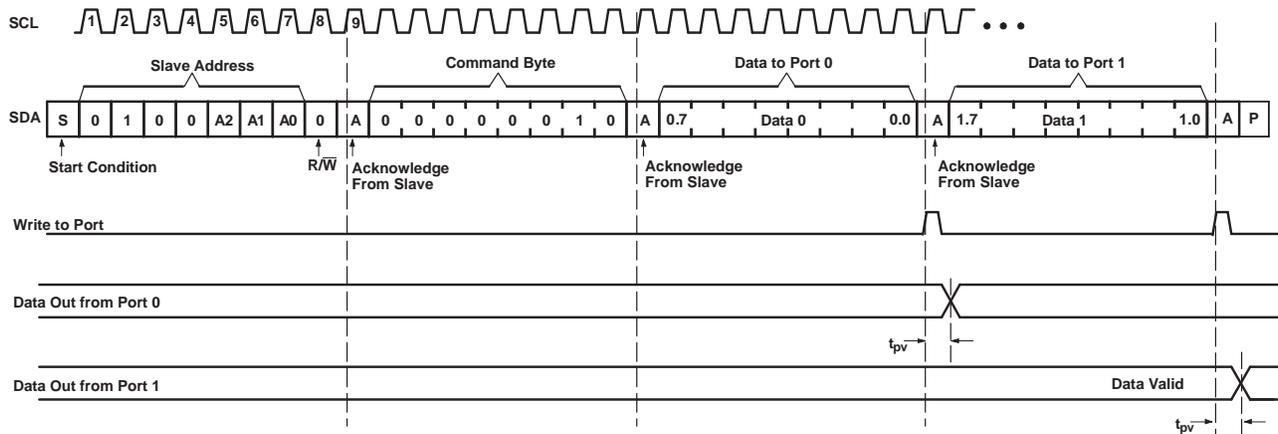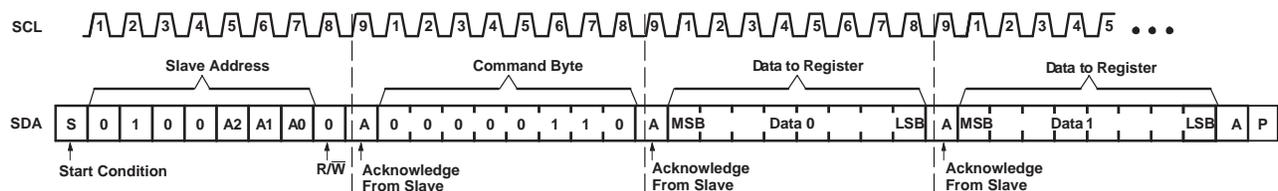

Figure 24. Write To Output Port Registers

Figure 25. Write To Configuration Registers

8.3.2.4.2 Reads

The bus master first must send the PCA9555 address with the least-significant bit set to a logic 0 (see Figure 22 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again, but this time, the least-significant bit is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9555 (see Figure 26 through Figure 28).

After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. For example, if the command byte references Input Port 1 before the restart, and the restart occurs when Input Port 0 is being read, the stored command byte changes to reference Input Port 0. The original command byte is forgotten. If a subsequent restart occurs, Input Port 0 is read first. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflect the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0.

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.
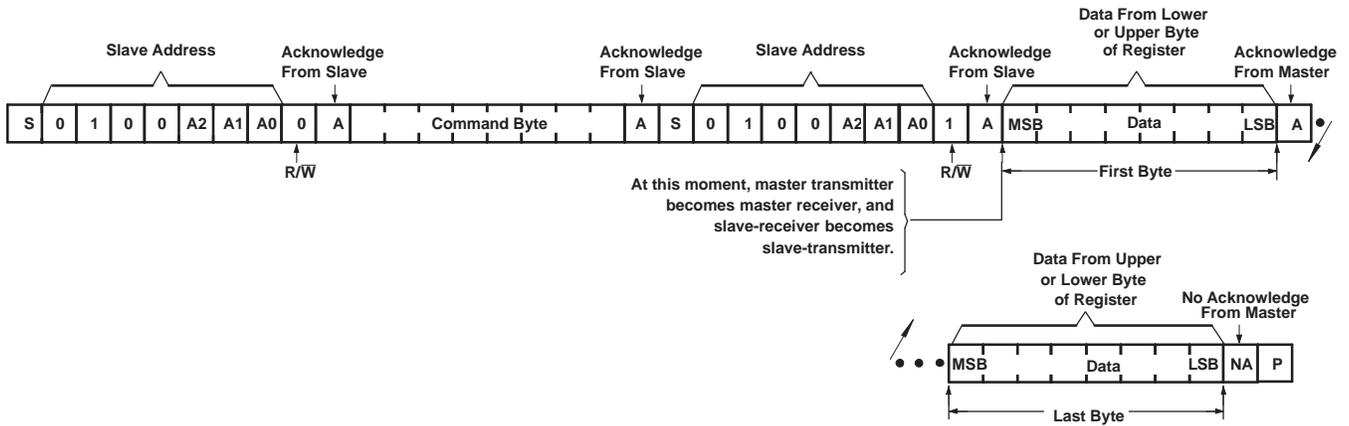
Figure 26. Read From Register

A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see Figure 26 for these details).

Figure 27. Read Input Port Register, Scenario 1
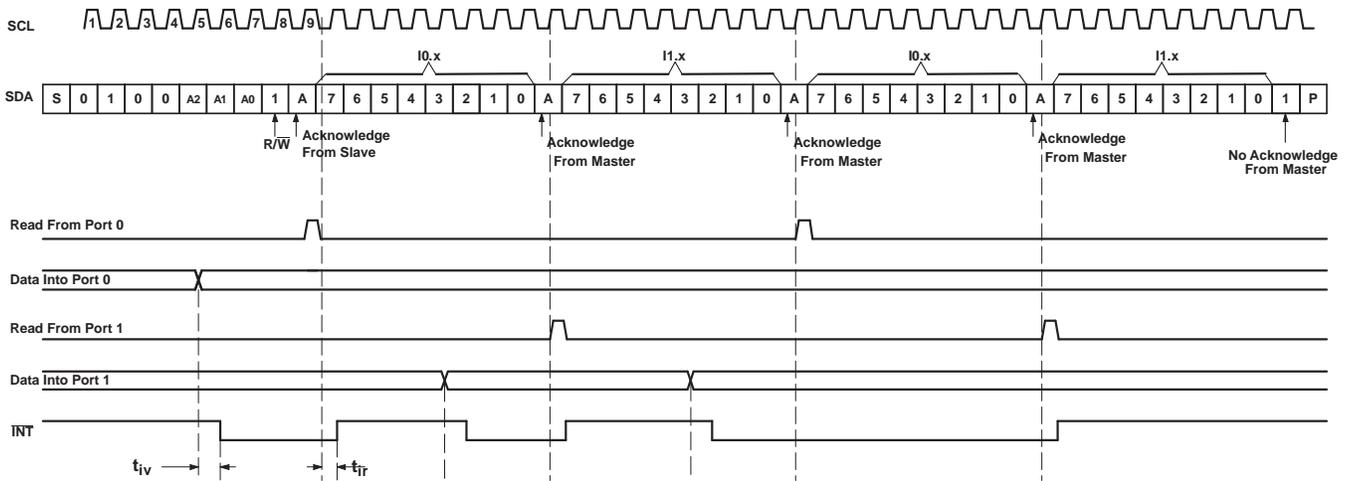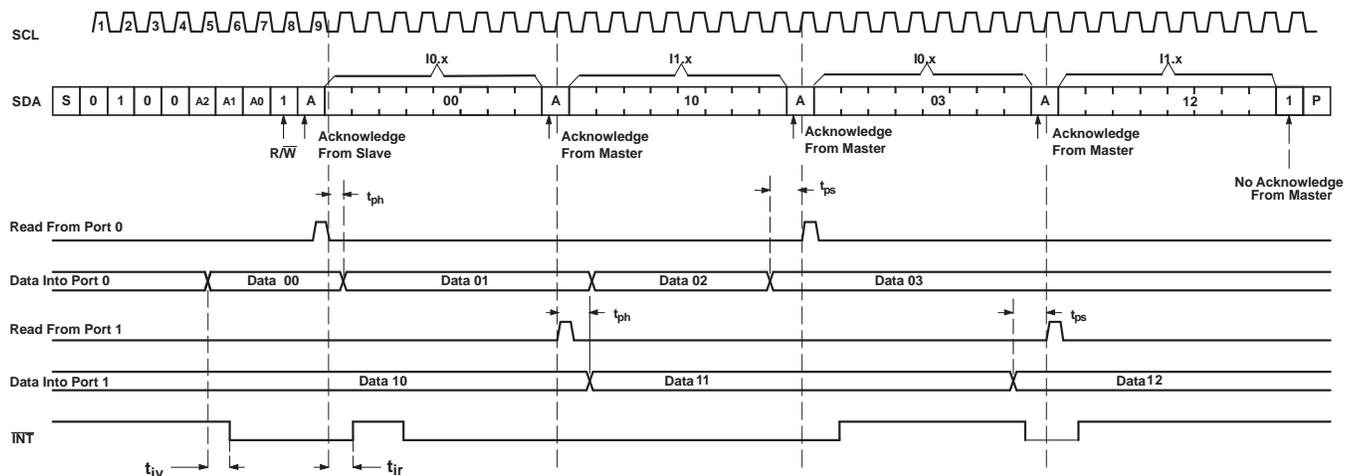
A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see Figure 26 for these details).

Figure 28. Read Input Port Register, Scenario 2

9 Application And Implementation

9.1 Typical Application

Figure 29 shows an application in which the PCA9555 can be used.
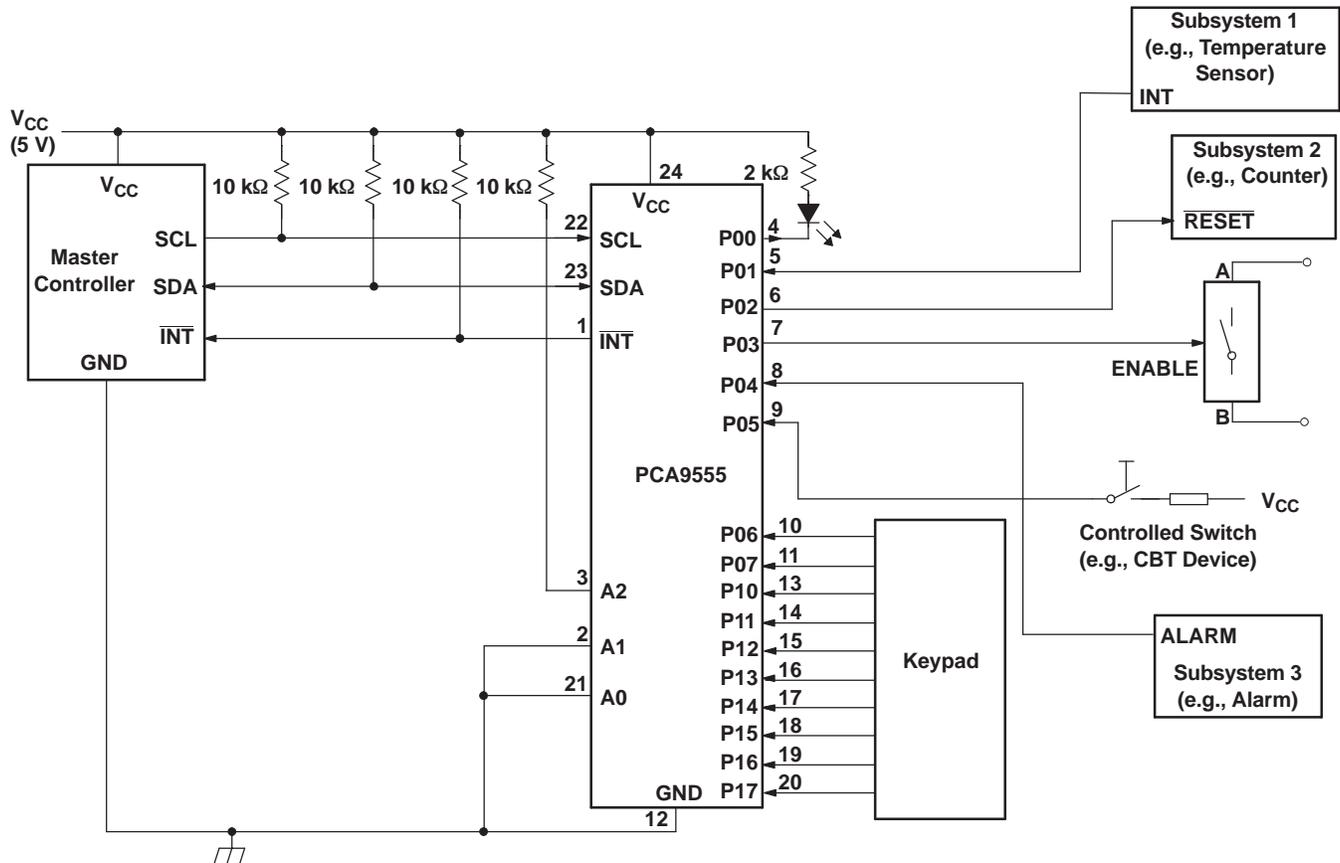
A. Device address is configured as 0100100 for this example.

B. P00, P02, and P03 are configured as outputs.

C. P01, P04–P07, and P10–P17 are configured as inputs.

D. Pin numbers shown are for DB, DBQ, DGV, DW, and PW packages.

Figure 29. Typical Application

Product Folder Links: *PCA9555*

Typical Application (continued)

9.1.1 Design Requirements

9.1.1.1 Minimizing I_{CC} When I/O Is Used To Control Led

When an I/O is used to control an LED, normally it is connected to V_{CC} through a resistor as shown in Figure 29. Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The ΔI_{CC} parameter in Electrical Characteristics shows how I_{CC} increases as V_{IN} becomes lower than V_{CC}. For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to V_{CC} when the LED is off to minimize current consumption.

Figure 30 shows a high-value resistor in parallel with the LED. Figure 31 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevent additional supply current consumption when the LED is off.
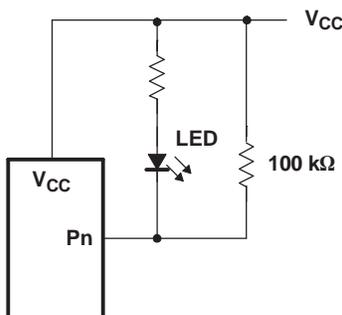

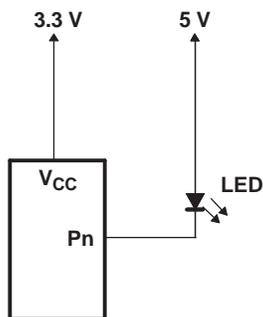**Figure 30. High-Value Resistor In Parallel With Led**

Figure 31. Device Supplied By Lower Voltage

Product Folder Links: *PCA9555*

10 Power Supply Recommendations

10.1 Power-On Reset Errata

A power-on reset condition can be missed if the VCC ramps are outside specification listed below.
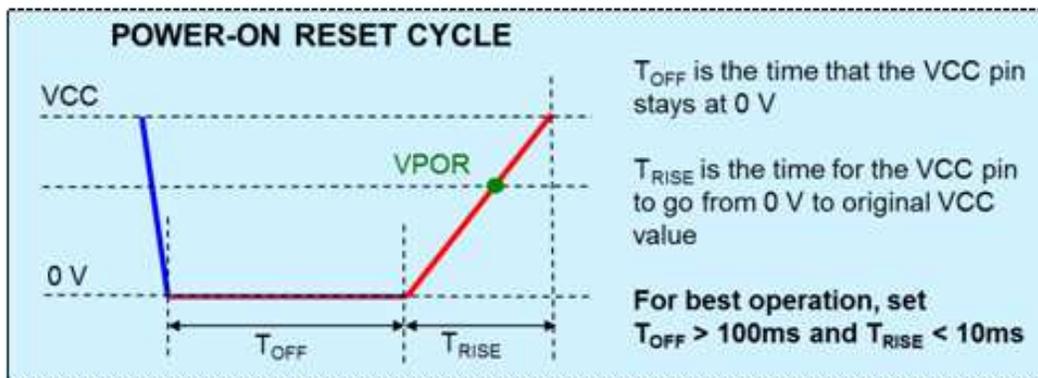
System Impact

If ramp conditions are outside timing allowances above, POR condition can be missed, causing the device to lock up.

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.
    This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9555DB	ACTIVE	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9555	Samples
PCA9555DBG4	ACTIVE	SSOP	DB	24		TBD	Call TI	Call TI	-40 to 85		Samples
PCA9555DBQ	NRND	SSOP	DBQ	24		TBD	Call TI	Call TI	-40 to 85		
PCA9555DBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PCA9555	Samples
PCA9555DBQRG4	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PCA9555	Samples
PCA9555DBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9555	Samples
PCA9555DBRG4	ACTIVE	SSOP	DB	24		TBD	Call TI	Call TI	-40 to 85		Samples
PCA9555DGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9555	Samples
PCA9555DGVRG4	ACTIVE	TVSOP	DGV	24		TBD	Call TI	Call TI	-40 to 85		Samples
PCA9555DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9555	Samples
PCA9555DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9555	Samples
PCA9555DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9555	Samples
PCA9555DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9555	Samples
PCA9555DWT	NRND	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 85		
PCA9555N	NRND	PDIP	N	24		TBD	Call TI	Call TI	-40 to 85		
PCA9555PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9555	Samples
PCA9555PWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9555	Samples
PCA9555PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9555	Samples
PCA9555PWR	NRND	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9555	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9555PWRE4	NRND	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9555	
PCA9555PWRG4	NRND	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9555	
PCA9555PWT	NRND	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		
PCA9555RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD9555	Samples
PCA9555RGERG4	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD9555	Samples
PCA9555RHLR	NRND	VQFN	RHL	24		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
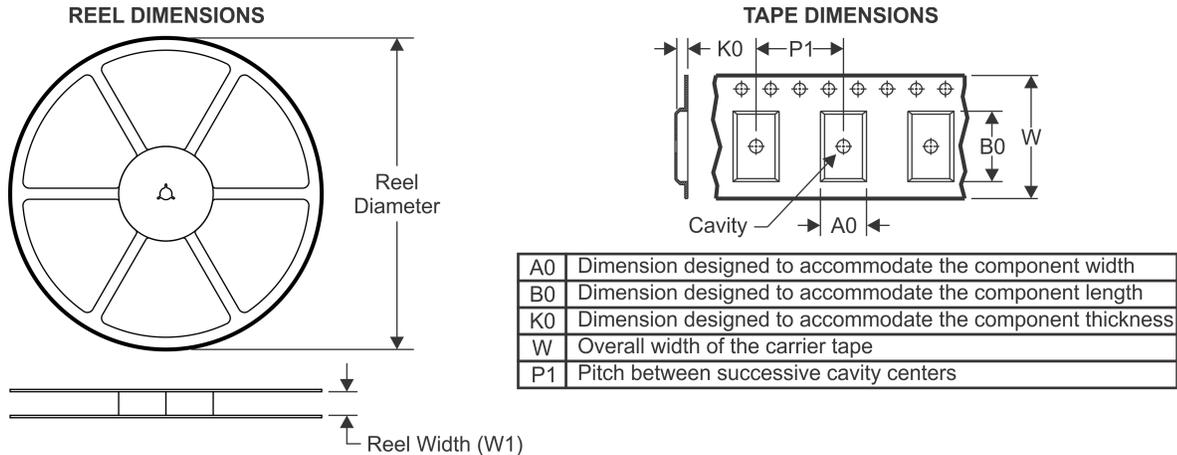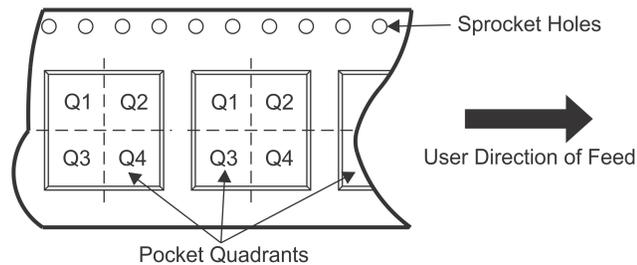
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

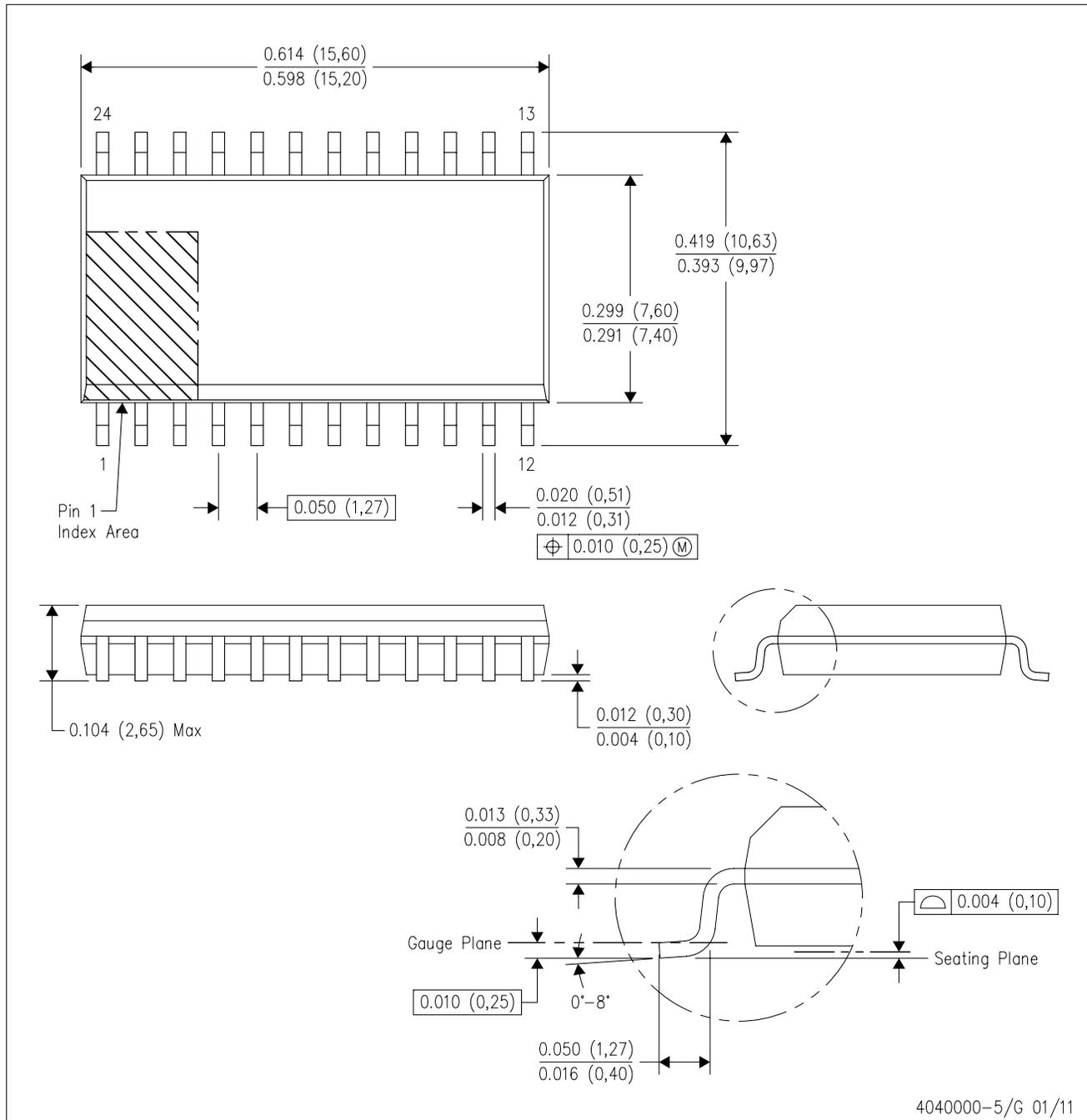| Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9555DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
PCA9555DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
PCA9555DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9555DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
PCA9555PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
PCA9555RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS
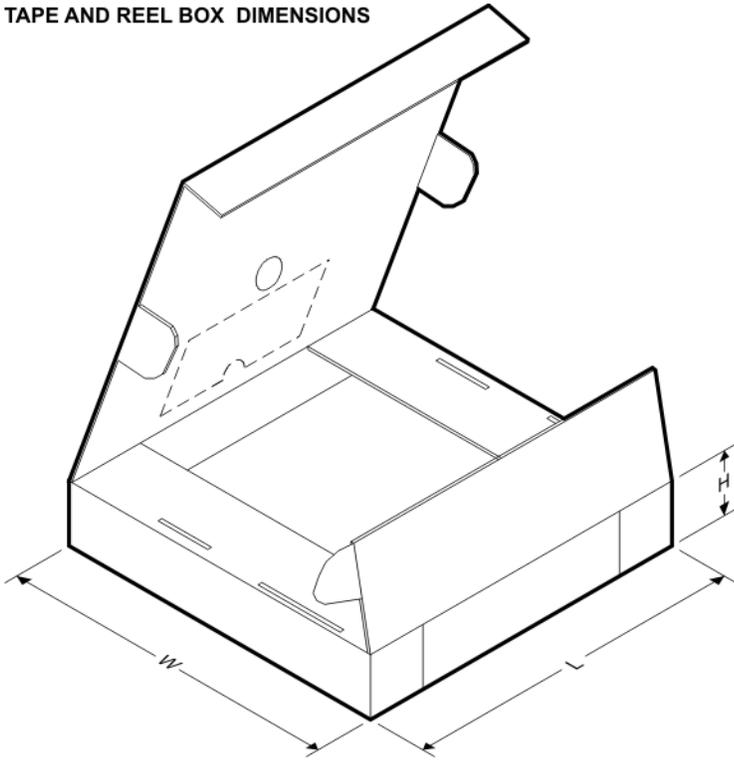
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9555DBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
PCA9555DBR	SSOP	DB	24	2000	367.0	367.0	38.0
PCA9555DGVR	TVSOP	DGV	24	2000	367.0	367.0	35.0
PCA9555DWR	SOIC	DW	24	2000	367.0	367.0	45.0
PCA9555PWR	TSSOP	PW	24	2000	367.0	367.0	38.0
PCA9555RGER	VQFN	RGE	24	3000	367.0	367.0	35.0

DW (R−PDSO−G24)   PLASTIC SMALL OUTLINE

0.614 (15,60)
0.598 (15,20)

24   13

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   12

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⌖ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

◠ | 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−5/G 01/11

NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−013 variation AD.
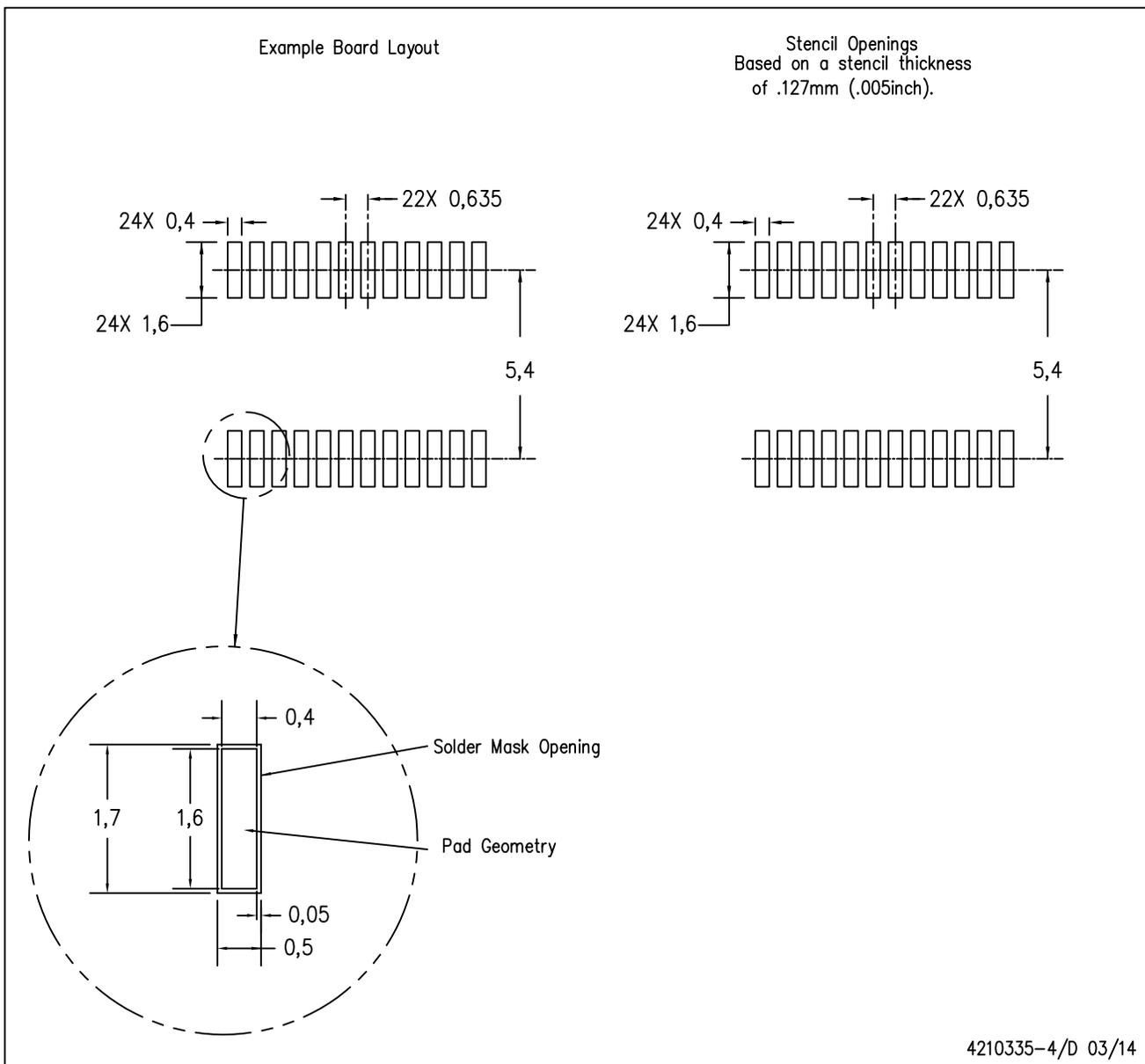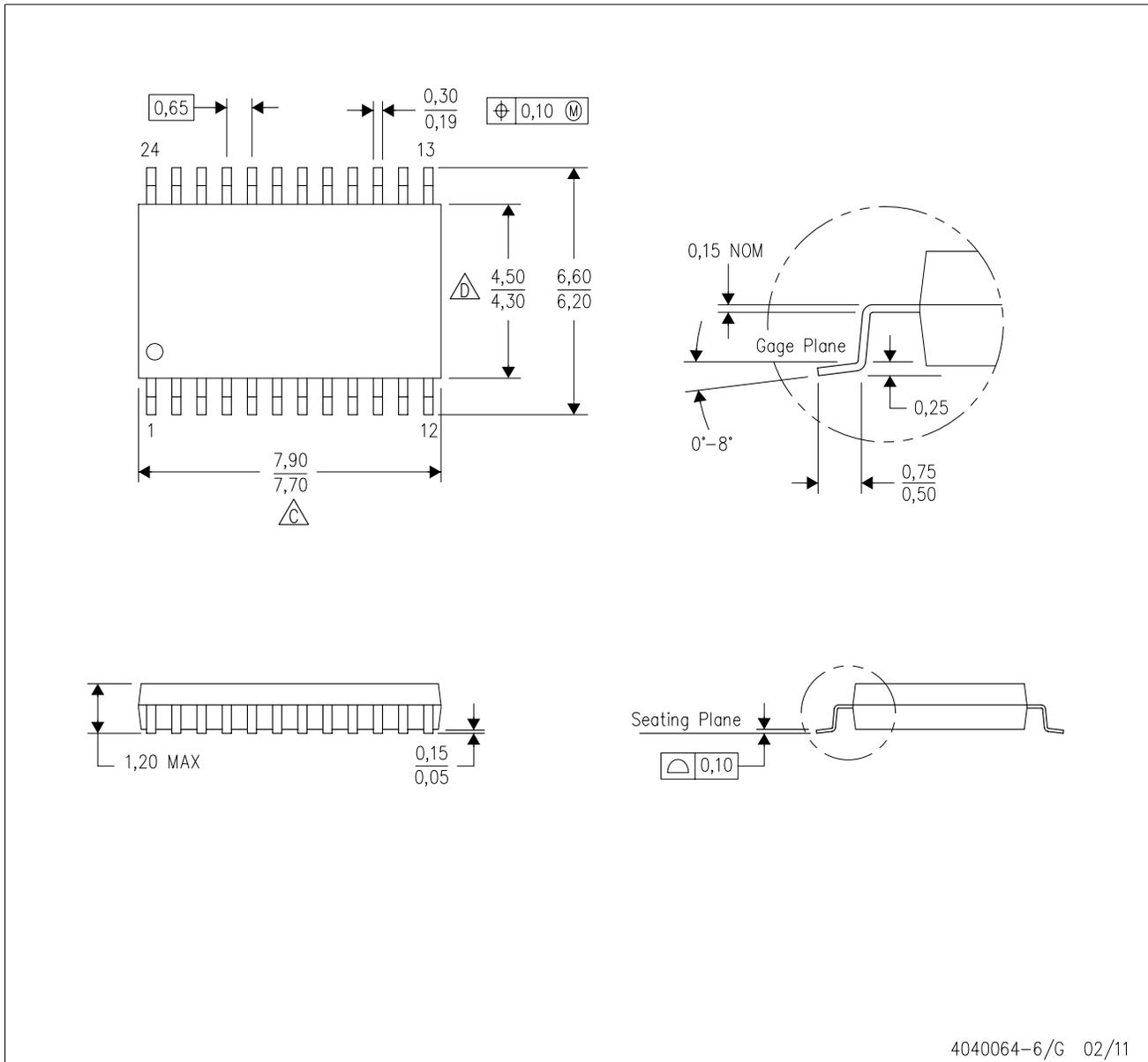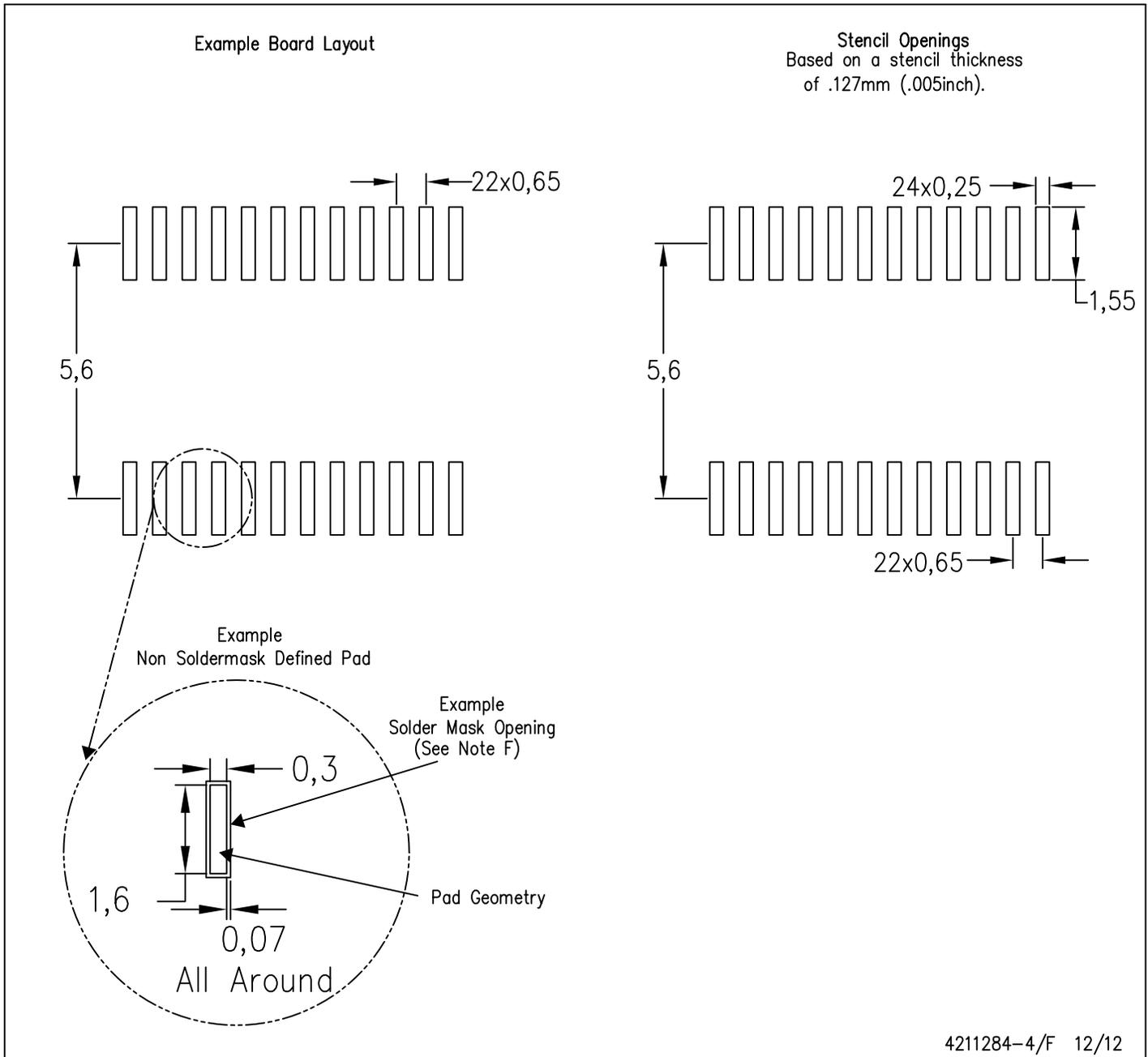
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DBQ (R−PDSO−G24)   PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

24   13

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1   12

Pin 1
Index Area

0.025 (0,635)

0.012 (0,30)
0.008 (0,20)

⊕ 0.005 (0,13) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.035 (0,89)
0.016 (0,40)

4073301−4/H 10/2008
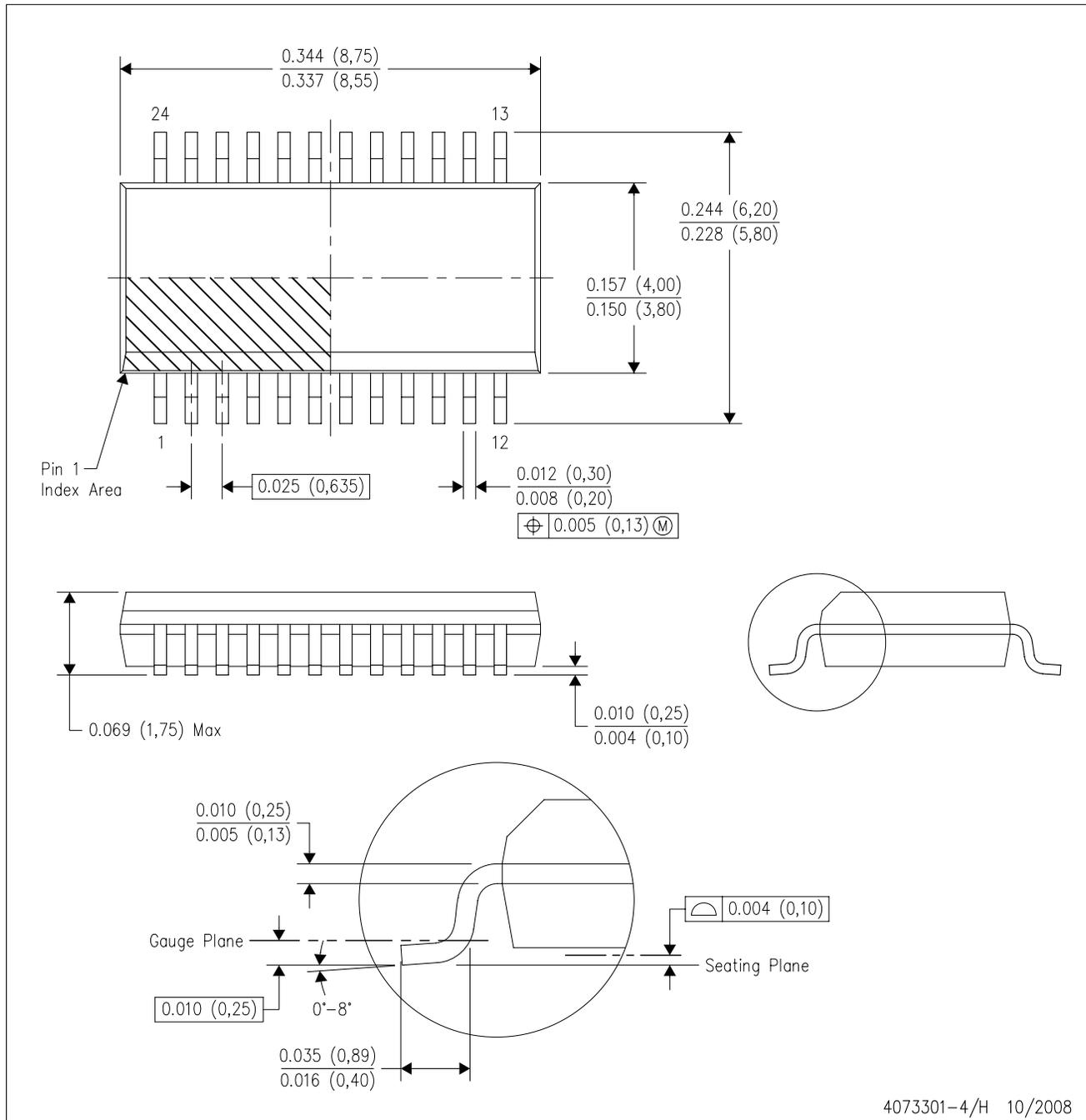
NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
        D. Falls within JEDEC MO−137 variation AE.

DBQ (R−PDSO−G24) PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

24X 0,4

22X 0,635

24X 1,6

5,4

24X 0,4

22X 0,635

24X 1,6

5,4

0,4

Solder Mask Opening

1,7 1,6

Pad Geometry

0,05

0,5

4210335−4/D 03/14
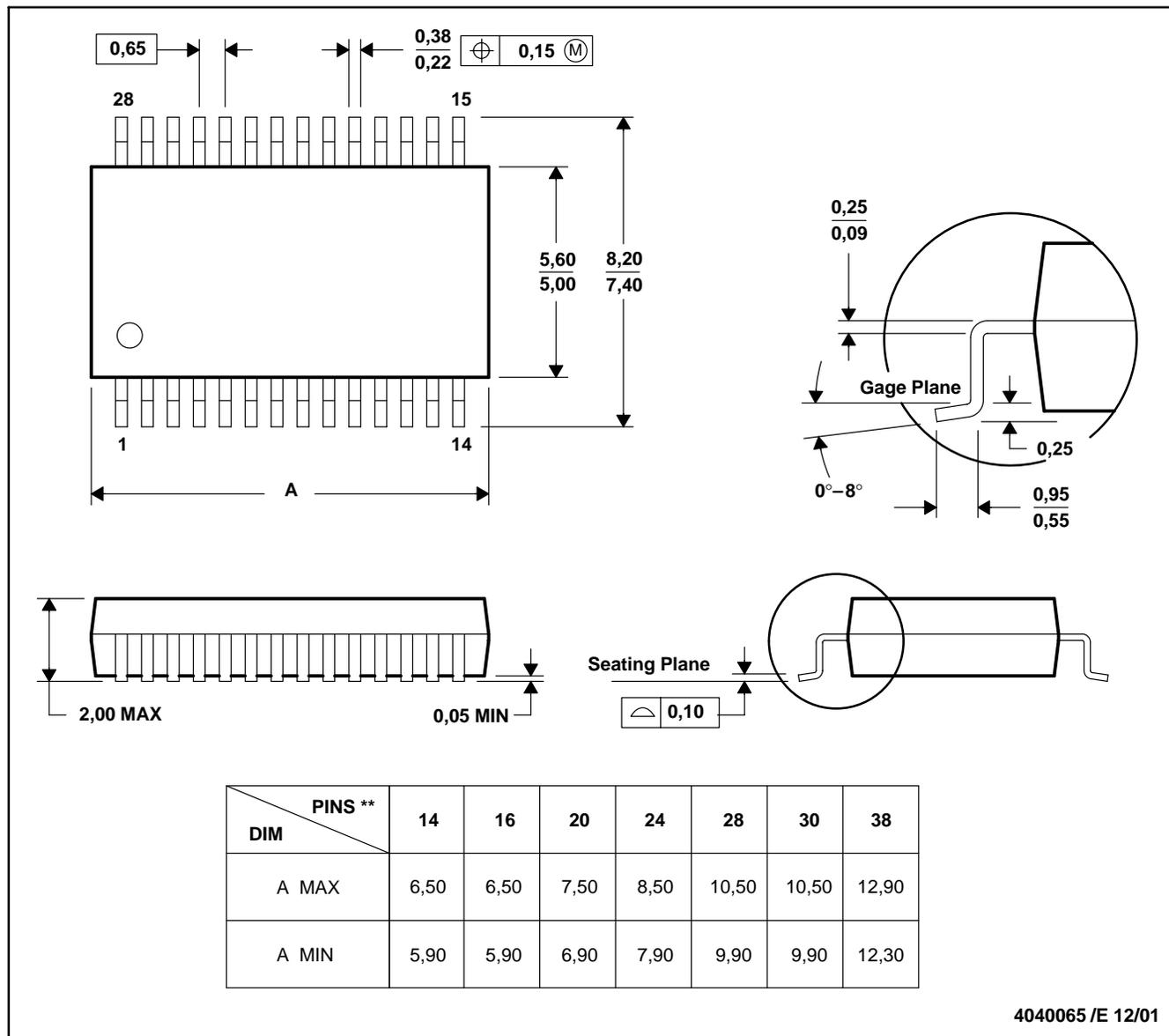
NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
            metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

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PW (R−PDSO−G24)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ | 0,10 Ⓜ

24   13

Ⅾ | 4,50
4,30

6,60
6,20

1   12

7,90
7,70

Ⅽ

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

◯ | 0,10

4040064−6/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B. This drawing is subject to change without notice.
         Ⅽ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0,15 each side.
         Ⅾ Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
         E. Falls within JEDEC MO−153

PW (R—PDSO—G24)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

22x0,65

24x0,25

1,55

5,6

5,6

22x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note F)

0,3

1,6

Pad Geometry

0,07
All Around

4211284—4/F   12/12

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC—7351 is recommended for alternate design.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC—7525 for other stencil recommendations.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
         D. Falls within JEDEC MO-150

RGE (S−PVQFN−N24)   PLASTIC QUAD FLATPACK NO−LEAD

$\frac{4,15}{3,85}$ A

B

$\frac{4,15}{3,85}$

PIN 1 INDEX AREA
TOP AND BOTTOM

$\frac{1,00}{0,80}$

0,20 REF.

SEATING PLANE

0,08

$\frac{0,05}{0,00}$ C

0,50   24X $\frac{0,50}{0,30}$

1   6

24   7

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

19   12

18   13   24X $\frac{0,30}{0,18}$

⊕	0,10 Ⓜ	C	A	B
	0,05 Ⓜ	C		

4204104/G 07/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Quad Flatpack, No−Leads (QFN) package configuration.
         D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
         F.   Falls within JEDEC MO−220.

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RGE (S−PVQFN−N24)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR (OPTIONAL)

1   6

24   7   Exposed Thermal Pad

2,10±0,10

19   12

18   13

2,10±0,10
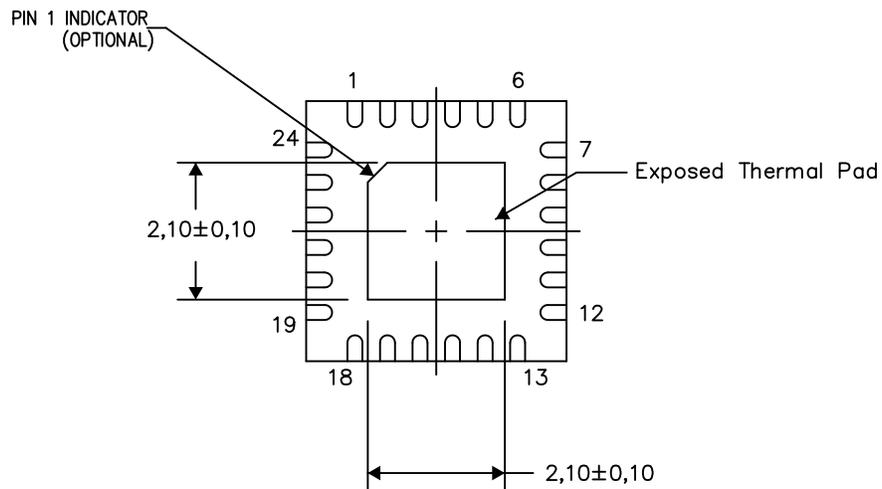
Bottom View

Exposed Thermal Pad Dimensions

4206344−6/AG 04/14

NOTES: A. All linear dimensions are in millimeters

RGE (S−PVQFN−N24)   PLASTIC QUAD FLATPACK NO−LEAD
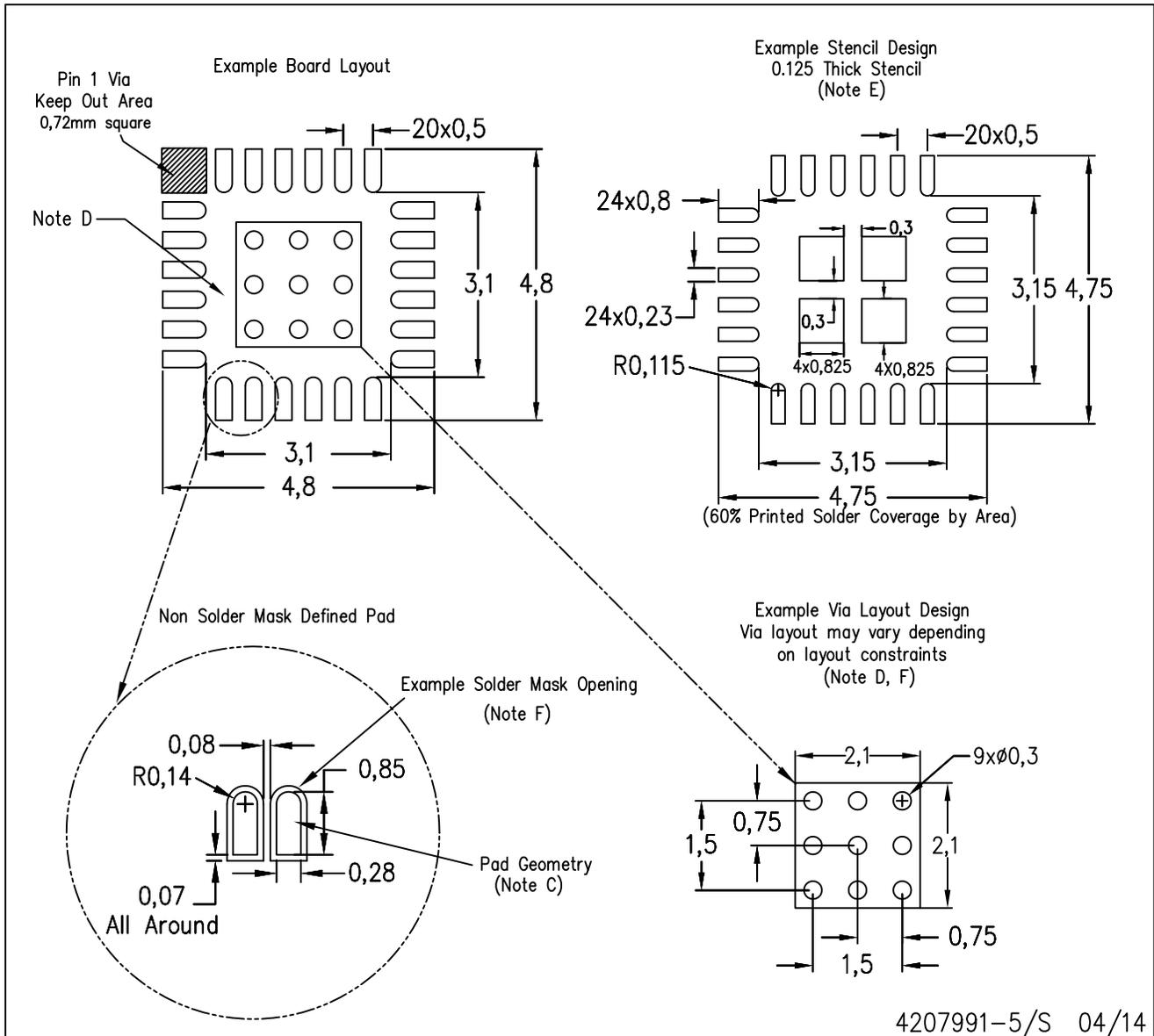
Pin 1 Via
Keep Out Area
0,72mm square

Example Board Layout

├── 20x0,5

Note D

3,1   4,8

3,1
4,8

Example Stencil Design
0.125 Thick Stencil
(Note E)

├── 20x0,5

24x0,8

0,3

24x0,23

3,15 4,75

0,3

R0,115

4x0,825   4X0,825

3,15

4,75
(60% Printed Solder Coverage by Area)

Non Solder Mask Defined Pad

Example Solder Mask Opening
(Note F)

0,08

R0,14   0,85

0,07   0,28
All Around

Pad Geometry
(Note C)

Example Via Layout Design
Via layout may vary depending
on layout constraints
(Note D, F)

2,1   9xØ0,3

0,75

1,5   2,1

0,75

1,5

4207991−5/S   04/14

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate designs.
         D.   This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack
              Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
              for specific thermal information, via requirements, and recommended board layout. These documents are available at
              www.ti.com <http://www.ti.com>.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design
              considerations.
         F.   Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting
              recommendations for vias placed in the thermal pad.

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RHL (R−PVQFN−N24)   PLASTIC QUAD FLATPACK NO−LEAD
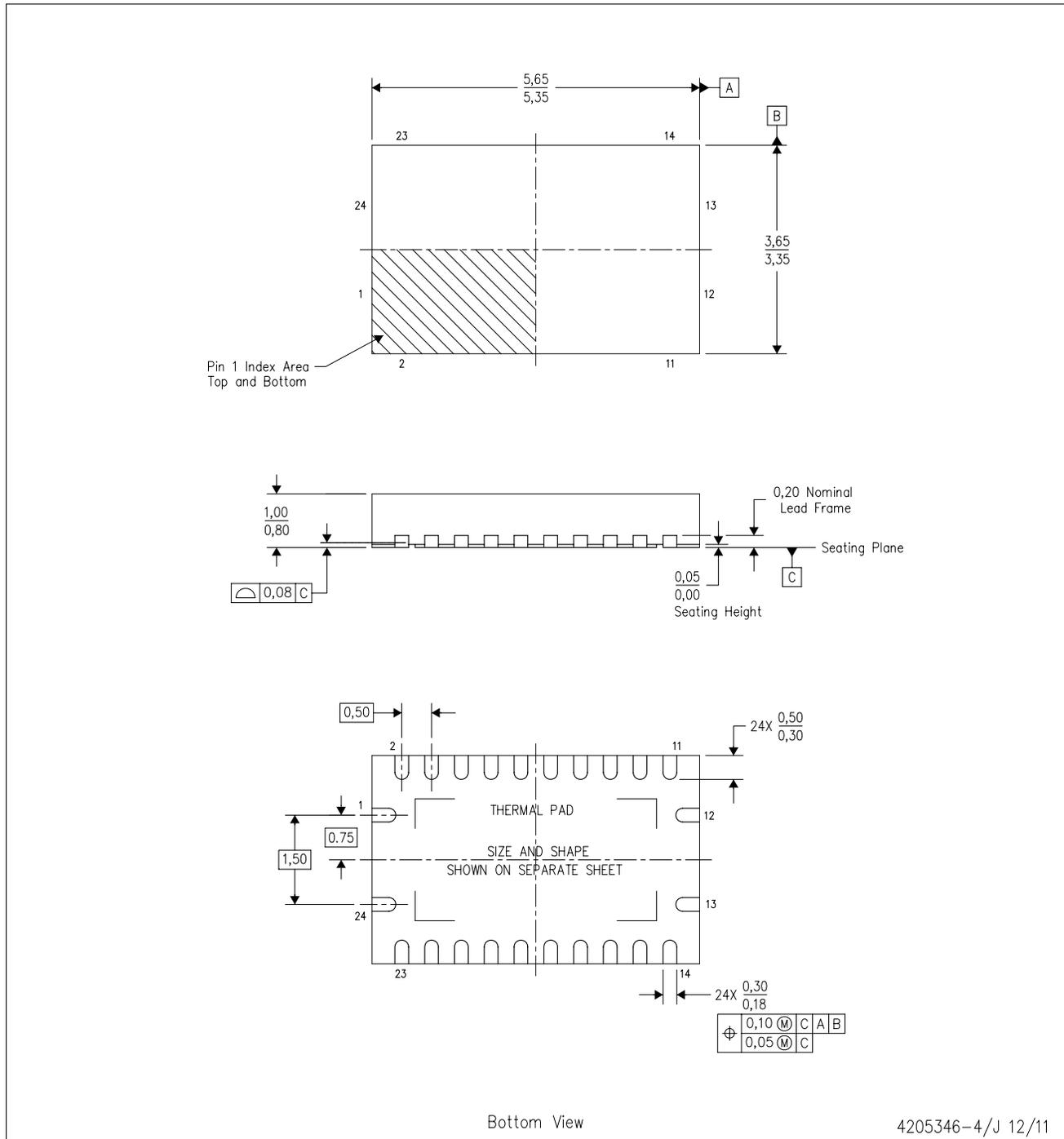
Pin 1 Index Area
Top and Bottom

$\frac{5,65}{5,35}$ A

B

$\frac{3,65}{3,35}$

0,20 Nominal
Lead Frame

Seating Plane

$\frac{1,00}{0,80}$

$\frac{0,05}{0,00}$
Seating Height

0,08 C

0,50

24X $\frac{0,50}{0,30}$

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

0.75

1,50

24X $\frac{0,30}{0,18}$

0,10 Ⓜ C A B
0,05 Ⓜ C

Bottom View

4205346−4/J 12/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   QFN (Quad Flatpack No−Lead) package configuration.
         D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
         F.   JEDEC MO−241 package registration pending.

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